09/518403

EXPRESS MAIL NO.: EL254108553US

DIGITAL RECORDING APPARATUS AND COPYRIGHT PROTECTION METHOD THEREOF

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a technique for processing copyright information in recording apparatus such as digital video cassette recorders (refer to as DVCR hereinafter) provided with a digital interface based on IEEE1394 format and computers.

Description of the Related Art

Commercial DVCRs which record/reproduce digitized video signals and audio signals have been commercially available. Such DVCR is provided with an interface for inputting and outputting video signals and audio signals as they are digital. Therefore, digital ~~doubling~~ dubbing is possible between DVCRs provided with a digital interface.

The digital interface described herein above is arranged in accordance with IEEE1394. In audio and video signal transmission protocol of IEEE1394, a digital interface transmits signals ~~to a transparent~~ in the clear based on the concept that transmission apparatus side and receiving side deal with copyright protection. Therefore a digital

interface transmits signals without copyright information.

Content sent by way of a digital interface is divided into two main classes, namely dynamic image signals and other signals (such as computer data and programs). It is required to manage copyright in all apparatus including computers in the case of dynamic image signals. However, in the case of an apparatus such as a computer in which data are writable using software, copy management information itself can be rewritten.

The present invention has been accomplished in view of such problem, ~~it is the~~ it is an object of the present invention to provide a method for protecting copyright in which an apparatus capable of rewriting copy management information such as a ~~computer can not~~ computer cannot accept signals other than copy free signals.

In order to solve the above-mentioned problem, the method for copyright protection in accordance with the present invention is the copyright protection method of digital signal to be inputted to a digital recording apparatus provided with a digital interface, in a header of a transmission frame of the digital signal to be transmitted a copyright protection information is contained, the copyright protection information restricts recording

of the digital signal to be inputted to the digital recording apparatus, wherein the copyright protection information includes the copy free information for indicating to the digital recording apparatus that the digital signal is copy free, and the information for indicating to the digital recording apparatus so that the digital recording apparatus performs copy management in compliance with the copyright information included in the content of the transmitted transmission frame.

A medium in accordance with the present invention is the medium which receives a content including a digital signal for performing copyright protection, in a header of a transmission frame of the digital signal to be transmitted a copyright protection information is contained, and the copyright protection information restricts recording of the digital signal to be inputted to the digital recording apparatus, wherein the copyright protection information includes the copy free information for indicating to the digital recording apparatus that the digital signal is copy free, and the information for indicating to the digital recording apparatus so that the digital recording apparatus performs copy management in compliance with the copyright information included in the content of the transmitted

transmission frame.

The digital recording apparatus in accordance with the present invention is the digital recording apparatus provided with a digital interface, wherein the digital recording apparatus has a means for detecting the copyright protection information provided in a transmission header of a transmission frame of a digital signal inputted through the digital interface, and a means for taking in the transmission frame and for allowing recording processing if the copyright protection information indicates copy free of the digital signal.

The control IC in accordance with the present invention is the control IC for controlling a link layer of a digital interface mounted on a digital recording apparatus provided with the digital interface, wherein the control IC has a means for detecting the copyright protection information provided in a transmission header of a transmission frame of a digital signal inputted through the digital interface, and a means for taking in the transmission frame and for indicating recording processing to the digital recording apparatus if the copyright protection information indicates copy free of the digital signal.

According to the present invention, a recording

apparatus which does not perform processing in compliance with the copyright information with a hardware accepts transmission frames only when the copyright protection information in a transmission header indicates copy free. A recording apparatus which performs processing in compliance with the copyright information with a hardware which accepts transmission frames when the copyright protection information in the transmission header indicates copy free, and when the copyright protection information in the transmission header indicates compliance with the copyright information contained in the content of the transmission frame, the copyright information in the content is fetched based on the signal format type information of the transmission header.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A and Fig. 1B are diagrams for illustrating the operation of a system to which the present invention is applied.

Fig. 2 is a diagram for illustrating the structure of the isochronous packet.

Figs. 3A and 3B are diagrams for illustrating format of a CIP header.

Fig. 4 is a diagram for illustrating the internal structure of a DVCR which is a CGMS acceptable apparatus including LINC and peripheral components.

Fig. 5 is a diagram for illustrating an ON-OFF switch portion actuated in response to the control performed by a copy free flag processing block for CGMS unacceptable apparatus.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described in detail hereinafter with reference to the drawings.

B. The present invention addresses on-line content (for example, software such as movie pictures and programs transmitted from satellite broadcasts, and software reproduced from media such as video tapes and video disks sold as rental video and video software.) which controls copyright information according to CGMS-D (Copy Generation Management System-Digital) system. An apparatus which can perform copyright protection management based on the management information defined by way of the CGMS-D system is referred to as CGMS acceptable apparatus, and an apparatus which has no function of copyright protection management

is referred to as CGMS-D unacceptable apparatus.

The CGMS-D system indicates copyright management condition using three codes. "00" indicates that the content is copy free, "11" indicates that the content is not copy free, and "10" indicates that the content can be copied only once.

The CGMS acceptable apparatus performs the processing "do not record if the apparatus detects that the content intended to be recorded is dynamic image signals and not allowed to be copied" using the above-mentioned code "00" by means of the hardware provided in the apparatus. The CGMS acceptable apparatus performs the processing "flag is changed to no copy flag and recording is performed if the apparatus detects that the content intended to be recorded is dynamic image signals and allowed to be copied once" using the above-mentioned code "10".

The CGMS unacceptable apparatus does not have a function to perform such processing. The apparatus which does not check the CGMS code by itself but instead uses built-in driver software that checks the CGMS code is not included in the category of CGMS acceptable apparatus. In other words, an apparatus in which the response to the CGMS is changeable depending upon ~~on a software such as a computer is categorized to the~~ CGMS

unacceptable apparatus.

The operation of a system to which the present invention is applied is shown in Figs. 1A and 1B. Fig. 1A shows a combination of a reproducer 1 and a CGMS acceptable recorder 2 connected with IEEE1394 serial bus 3, and Fig. 1B is a combination of a reproducer 1 and a CGMS unacceptable recorder 4 connected with IEEE1394 serial bus. Herein, the reproducer includes not only a DVCR described herein above but also a digital television tuner and digital television receiver having function to receive digital television broadcast and output digital video signals and digital audio signals to IEEE1394 serial bus.

As shown in Fig. 1A, in the case that the recorder is CGMS acceptable, the transmitted signal can be accepted, and on the other hand, in the case that the recorder is CGMS unacceptable as shown in Fig. 1B, the transmitted signal can not be accepted by the digital interface (herein, IEEE1394 interface) though the signal in Fig. 1B is the same as the signal in Fig. 1A.

A transmission frame (isochronous packet) transmitted to IEEE1394 serial bus has the structure as shown in Fig. 2, in the case that real time data such as digital audio signals or digital video signals are transmitted, a

header referred to as CIP header is added. The format of a CIP header is shown in Figs. 3A and 3B. Fig. 3A shows a CIP header with a time sump (SYT) and Fig. 3B shows a CIP header without a time sump (SYT).

In this embodiment, copyright protection information is added to the digital video signal having the isochronous packet type structure using the reserved area (rsv) (2 bits) of a CIP header as described in (1) and (2) herein under in detail.

(1) A bit which indicates copy free and flag of CGMS-D contained in the content are detected, and a bit which indicates that the recording apparatus should follow the indication is assigned respectively.

(2) Only 1 bit is used, and 0 indicates copy free and 1 indicates that a flag of the CGMS-D in the content is detected and an indication that the apparatus should perform in compliance with the indication is given to the recording apparatus.

In detail, in the case that the recorder is a CGMS acceptable apparatus, if the bit of the reserved area of the CIP header is a bit which is in the condition that indicates copy free, the recorder accepts the data of the content as it is. A flag of CGMS-D is detected, and if the

flag is a flag which is in the condition that indicates compliance with the CGMS-D, the recording apparatus accepts the flag of CGMS-D and performs processing of the copy management in compliance with the CGMS-D. Herein, because the location where a flag of CGMS is contained is different depending on the type of the signal transmitted on the IEEE1394 serial bus, the type of the signal is judged based on the FMT (format field) of the CIP header and the location of the flag is confirmed. For example, a flag of a CGMS is located in a VAUX (video auxiliary data) in the case of reproduction signals of DVCR (SD, HD), differently, a flag of a CGMS is located in a PES header in the case of receiving signal of digital broadcast such as DirecTV and DVB.

A recorder that is a CGMS unacceptable apparatus accepts it as it is if the bit of the reserved area of a CIP header is a bit which is in the condition that indicates copy free. The recorder does not accept the input data content if the flag of CGMS-D is detected, and the flag is a flag which is in the condition that indicates the recording apparatus to perform compliance with CGMS-D.

In both cases of a CGMS acceptable apparatus and CGMS unacceptable apparatus, the hardware of link layer control IC of the IEEE1394 interface performs the above-mentioned

processing. In other words, copyright protection is performed by the digital interface using the link layer control IC for a CGMS acceptable apparatus or using the link layer control IC for a CGMS unacceptable apparatus.

Fig. 4 shows the internal structure of a DVCR which is a CGMS acceptable apparatus including a link layer control IC (hereinafter referred to as LINC ~~refer to as LINC hereinafter~~) with peripheral components. The DVCR is provided with a physical layer control IC (hereinafter referred to as PHY ~~refer to as PHY hereinafter~~) 1, a LINC 2, a microprocessor 3, a digital VCR signal processor 4, and PLL 5.

PHY 1 performs initialization of the bus and conciliation of usufructuary right. PHY 1 communicates data such as digital video signals and various control signals (control) with LINC 2, and transmits these data and control signals to the cable. Further PHY 1 supplies a system clock (sysclk) to LINC 2. Details of LINC 2 is described hereinafter. The microprocessor 3 performs control of PHY 1 and LINC 2 and acquisition of an isochronous communication band. The digital VCR signal processing system 4 records/reproduces digital video signals and digital audio signals. PLL 5 receives frame synchronizing information from LINC 2 and generates clock signals (clk), and supplies them to LINC 2 and the digital VCR signal processor 4.

The internal structure of LINC 2 is divided into three main blocks, an isochronous system, an asynchronous system, and a basic block. The isochronous system is a block for generating and analyzing isochronous packets on which data such as digital video signals are loaded, and the asynchronous system is a block for generating and analyzing asynchronous packets on which control signals such as commands for controlling apparatus are loaded.

The asynchronous system comprises a microprocessor interface 6, control register 7, asynchronous packet transmission FIFO 8, asynchronous packet reception FIFO 9, and self ID packet processing block 10.

Basic block 11 is provided with a clock, CRC, physical interface, transmission block, and receiving block.

The isochronous system comprises a digital signal processing interface 12, isochronous packet transmission receiving FIFO 13, header and synchronous information adding circuit 14, header removing and synchronous information restoration circuit 15, copy free flag processing block 16, CGMS processing block 17, and switch SW.

The microprocessor interface 6 transmits to and receives from the microprocessor 3 the data corresponding to the request from the high order layer.

The microprocessor 3 writes data in the control register 7 at the predetermined position to control the operation of LINC 2. While asynchronous packets are transmitted or received, this operation is performed by reading or writing the predetermined address. Further, the partial header of the isochronous packet is transmitted or received through this register.

The asynchronous packet transmission FIFO 8 temporarily stores the packet generated by the microprocessor 3. The stored packet is read by the basic block 11 immediately when the bus becomes free.

The basic block 11 writes the packet transferred from the bus in the asynchronous packet receiving FIFO 9. The microprocessor 3 reads it after confirming that the FIFO 9 is not free.

The self ID packet processing block 10 performs processing of node information received during initialization of the bus, and detects the number of nodes connected to the bus and the node that controls the isochronous channel of the bus.

The physical interface of the basic block 11 performs parallel/serial conversion of transmission data and serial/parallel conversion of reception data. The

transmission block judges condition of the bus, and controls transmission of the packet. The reception block determines a component to be written depending on the type of the received packet (asynchronous or isochronous).

The digital signal processing interface 12 converts data of the digital VCR signal processing system 4 to data of the isochronous packet format while transmitting, and converts inversely while receiving.

The isochronous packet transmission reception FIFO 13 is a FIFO which functions also to transmit/receive an isochronous packet, the packet is read by the basic block 11 as long as the packet is read while transmitting, and the packet is written as long as the FIFO does not overflow while receiving.

The header and synchronous information adding circuit 14 writes the information specified by the IEEE1394 in the header portion (before the data field in Fig. 2). Further the header and synchronous information adding circuit 14 digitizes the frame synchronous signal of a video signal to be transmitted based on the clock in the basic block 11, and writes it in a specified packet.

The header removing synchronous information restoration circuit 15 removes information from the header,

thereafter writes only data in the isochronous packet transmission reception FIFO 3. Further, the header removing synchronous information restoration circuit 15 transmits the bit in the reserved area in a CIP header to the copy free flag processing block 16. Further, the header removing synchronous information restoration circuit 15 restores the frame synchronous signal from the digitized frame synchronous information written in a specified packet based on the clock in the basic block 11.

The copy free flag processing block 16 switches the switch SW to the terminal-a side if the bit in the reserved area received from the header removing and synchronous information restoration circuit 15 indicates ~~free copy~~ copy free, and switches to the terminal-b side if the flag is detected and the flag indicates compliance with the CGMS-D.

The CGMS processing block 17 separates FMT in a CIP header from a digital video signal which is outputted from the digital signal processing interface 12 and inputted through the switch SW, and sends it with the digital video signal and digital audio signal to the digital VCR signal processing system 4.

Therefore, if the bit of the reserved area in a CIP header indicates compliance with the CGMS-D with reference

to the flag of CGMS-D, a digital video signal and digital audio signal are supplied from the digital signal processing interface 12 to the digital VCR signal processing system 4, and FMT is supplied from the CGMS processing block 17. The digital VCR signal processing system 4 identifies the location where the CGMS flag is located based on FMT (which is VAUX data if it is a reproduction signal of DVCR, and which is PES header if it is a digital television broadcast signal), and performs recording processing according to the CGMS flag.

To the contrary, if the bit of the reserved area in the CIP header indicates copy free, only the digital video signal and digital audio signal are supplied from the digital signal processing interface 12 to the digital VCR signal processing system 4, and the digital VCR signal processing system 4 performs recording processing as it is.

The CGMS acceptable apparatus is described hereinbefore with reference to Fig. 4. On the other hand, the CGMS processing block 17 is removed from Fig. 4, the signal line between the digital signal processing interface 12 and digital VCR signal processing system 4 is changed to a two-way signal line, and a switch SW which is turned ON/OFF by the copy free flag processing block 16 is provided

on the two-way signal line, and thereby a CGMS unacceptable apparatus is structured. (Fig. 5)

In the above-mentioned embodiments, copyright protection information is provided in rsv area of a CIP header, however it is possible to provide copyright protection information in an area other than rsv area (for example, sy area in a header information)

As described hereinbefore, according to the present invention only the apparatus which performs correct copy management can accept and record signals from the digital interface.